New Release

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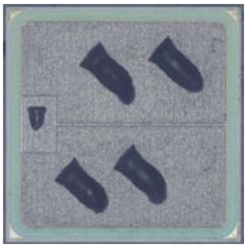
SiC MOSFET(1200V): SMC Diode Solutions S2M0080120D Overview and Structure Analysis Report

Package



SiC MOSFET die

Overview

SMC Diode Solutions is a US-funded semiconductor design and manufacturing company based in Nanjing, China, and started the operation of power discrete factory in Nanjing, in 2024 to strengthen sales of SiC devices in China. The company is a manufacturer that designs and manufactures discrete semiconductors, mainly diodes for consumer products. LTEC released the structure analysis report of its 1200V SiC MOSFET for automotive in order to understand its technological capabilities in automotive product.

Product features

- Product number: S2M0008120D V_{DSS} = 1200V, I_D = 41A, $R_{DS(on)}$ = 77mΩ
  Product release data: July 2023
- SMC's first generation SiC MOSFET.
- Application: EV fast charging module, EV on-board charger, solar inverter, DC-DC converter

Report Contents (Please refer to P.2,3 for the table of contents of each report.)

1. Overview Analysis Report (12 pages)

- Observation of package and SiC MOSFET die, cross-section analysis of die cell and edge

2. Structure Analysis Report (68 pages)

- A very thin and flat die attach (Pb-based) is used.
- The cell array has a planar gate structure.
- A JTE and a guard ring (inside the JTE) are formed on the outer periphery of the die to reduce the electric field strength.
- Compared to the STMicro's 1200V SiC MOSFET , a major manufacturer, the performance (RonAA) is inferior, but it is comparable to the products from BASiC Semiconductor, a major Chinese manufacturer.

Report price

Delivered one week after order placement

Please contact us for report pricing.

Report No : 23R-1005-1,2
Release day : 2024.06.21

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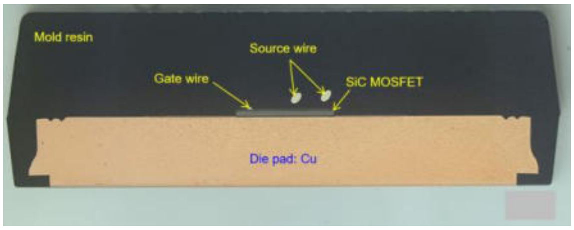
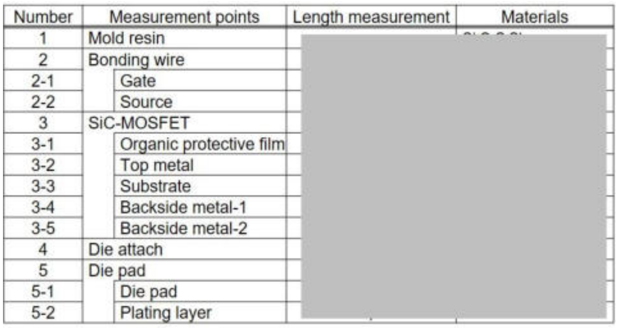
Excerpt from (2) Structure analysis report

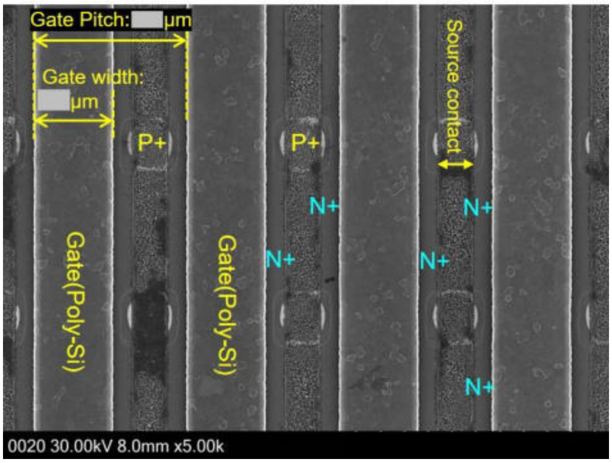


Package cross-sectional structure

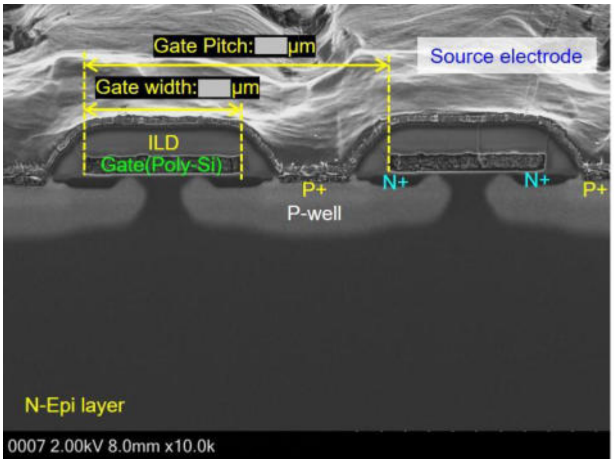


Number	Measurement points		Length measurement	Materials
1	Mold resin		[redacted]	[redacted]
2	Bonding wire		[redacted]	[redacted]
2-1		Gate	[redacted]	[redacted]
2-2		Source	[redacted]	[redacted]
3	SiC-MOSFET		[redacted]	[redacted]
3-1		Organic protective film	[redacted]	[redacted]
3-2		Top metal	[redacted]	[redacted]
3-3		Substrate	[redacted]	[redacted]
3-4		Backside metal-1	[redacted]	[redacted]
3-5		Backside metal-2	[redacted]	[redacted]
4	Die attach		[redacted]	[redacted]
5	Die pad		[redacted]	[redacted]
5-1		Die pad	[redacted]	[redacted]
5-2		Plating layer	[redacted]	[redacted]

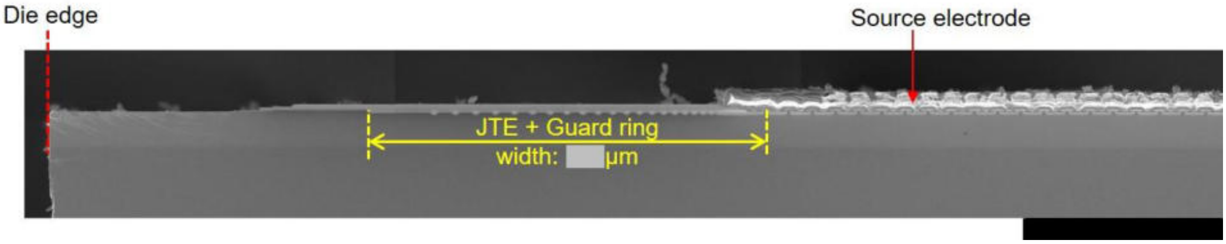
Package cross-sectional structure overview



Plane SEM image of cell array (Poly-Si layer)



Cross-sectional SEM image of cell array



Cross-sectional SEM image of the die outer periphery