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SiC MOSFETs (650V-1700V) : Epi (Drift+Buffer) Layer Survey Report

Overview

In SiC devices, in addition to determining the maximum operating and breakdown voltages, the structure and engineering of the SiC Epitaxial layer contains a significant amount of know-how to mitigate the adverse effects of crystal defects in the surface-active layer of vertical transistors. Since SiC substrates are not yet standardized, almost every SiC device manufacturer prepares the Epi layer with its own recipe, and the structure of each Epi layer is different (see P.3).

◆ Based on the data we have collected (SEM, SCM, etc.), this survey report presents:

1) Types of Epi layer/Buffer layer structures used by major manufacturers
2) Details of Epi layers for patent certification
3) Comprehensive academic and industrial references overview
4) Impact of Epi layers on manufacturing costs

Product features

	Maker	Product		Epi layer features
1	INFINEON	IMBG120R078M2H	Gen 2	N-buffer doping profile
2	NEXPERIA	NSF080120L3A0		Made by Mitsubishi Electric (estimated) Very thick buffer layer
3	Onsemi	NTH4L028N170M1	M1	two-layer N-Buffer
4	STMicro	SCT040H65G3AG or SCT040W120G3AG	Gen 3	Extremely thin N-Buffer

Report contents and Summary of results (42 pages)

The table of contents and excerpts from this report are listed on the following pages.

- Extraction and comparison of N-Buffer structures for preventing BPD (Basal Plane Dislocation) from major SiC manufacturers.
- The thickness of the N-Buffer layer varies greatly depending on the manufacturer, ranging from 0.4 µm to over 10 µm.
- The carrier concentration of each layer is extracted by SEM and SCM analysis, and the doping of the N-Buffer layer is 1E17 to 1.5E18 at/cm3.
- The cost of the Epi layer is estimated to be as much as 120% of the cost of a raw SiC substrate wafer (150 mmΦ) for a thick Epi layer.
- A "screening" test is considered necessary to supplement the N-Buffer layer.

Report price

Delivered one week after order placement

Please contact us for report pricing.

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Excerpt from the report (1)

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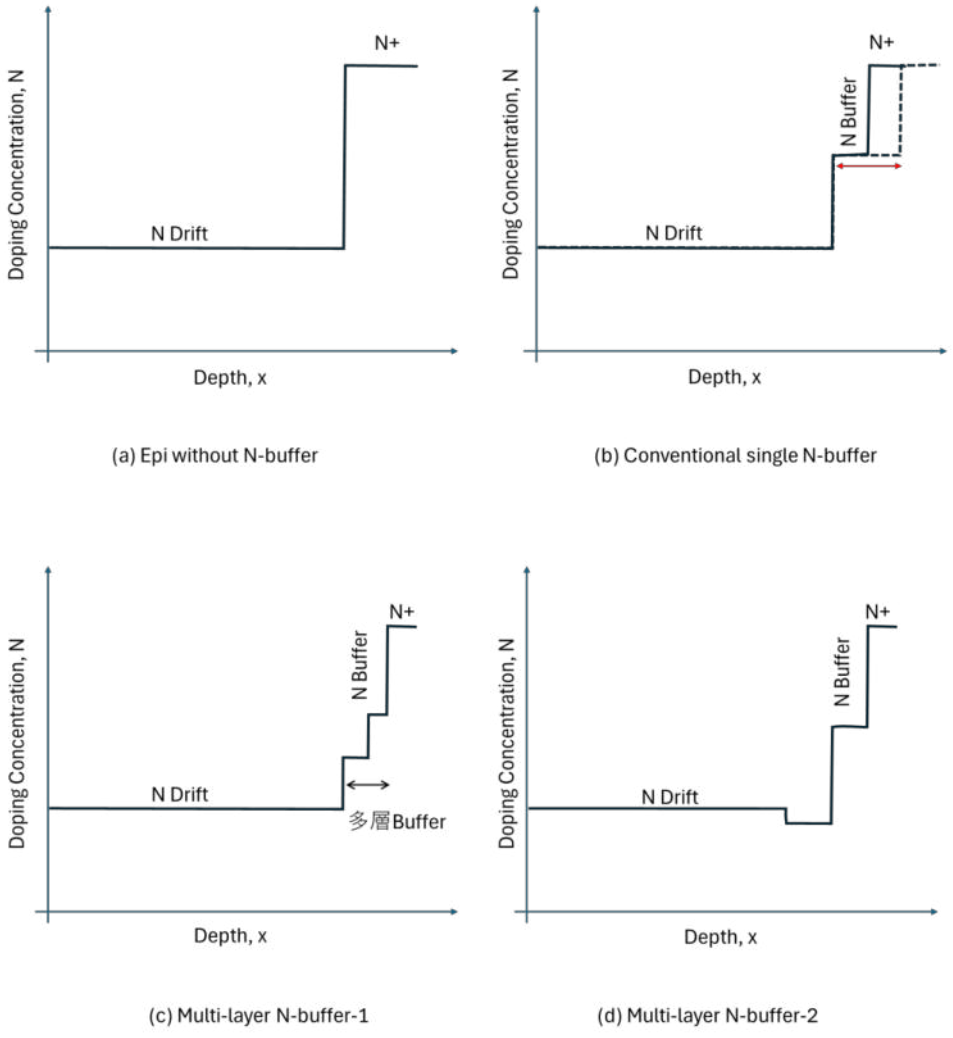
Excerpt from the report (2)

Epitaxial layer engineering



Example doping profile of SiC Epi (Drift and N-Buffer) layers in SiC power devices

Excerpt from the report (3)

Table 2-1-1: SiC MOSFET structure die and Epi layers comparison

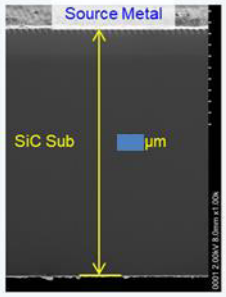
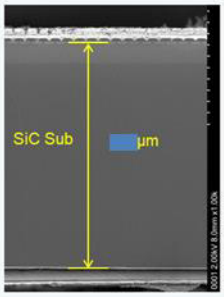
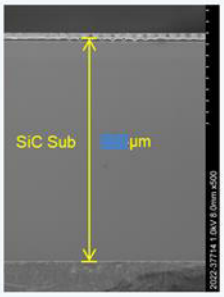
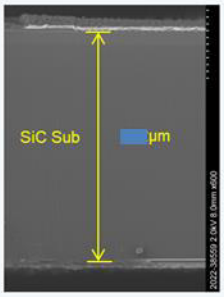
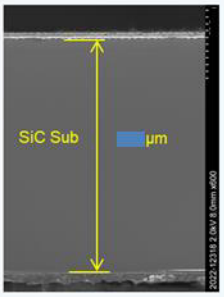
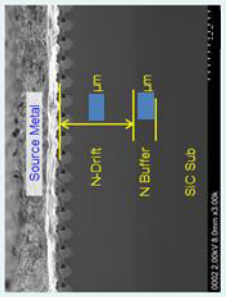
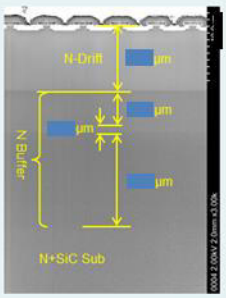
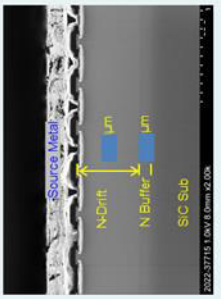
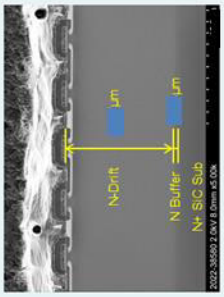
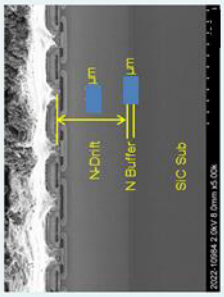
	Infineon IMBG120R078M2H	NEXPERIA NSF080120L3A0	Onsemi NTH4L028N170M1	STMicro SCT040W120G3AG	STMicro SCT040H65G3AG
V_{dss}	1200 V	1200 V	1700 V	1200 V	650 V
Die Thickness					
Epi Layer					

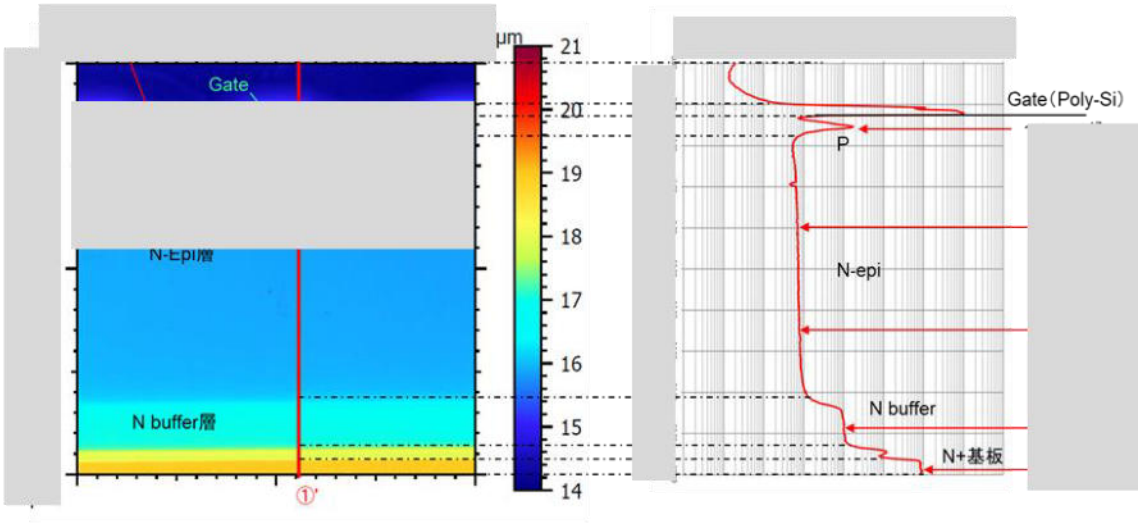
Table 2-1-2: Summary of the features of the Epi layer structure of the evaluated SiC MOSFETs

		INFINEON	NEXPERIA	onsemi	STMICRO	STMICRO
		Gen 2 CoolSiC		M1	Gen 3	Gen 3
Product		IMBG120R078M2H	NSF080120L3A0	NTH4L028N170M1	SCT040W120G3AG	SCT040H65G3AG
Device: Diode/Transistor ?		MOSFET	MOSFET	MOSFET	MOSFET	MOSFET
Vdss	V	1200	1200	1700	1200	650
Ron	mΩ	78.1	80	28	40	40
Transistor structure		Asymm. Trench	Planar Gate	Planar Gate	Planar Gate	Planar Gate
Die thickness	µm					
N drift thickness, Xd	µm					
N Buffer-1 thickness, Xb1	µm					
N Buffer-2 thickness, Xb2	µm					
N Buffer-3 thickness, Xb3	µm					
N drift Carrier Concentration, Nd	at/cm3					
N Buffer-1 Carrier Concentration, Nb1	at/cm3					
N Buffer-2 Carrier Concentration, Nb2	at/cm3					
N Buffer-3 Carrier Concentration, Nb3	at/cm3					
N+ Sub Carrier Concentration, Nsub	at/cm3					
※ Notable feature						
RonA	mΩ·mm²					
RepiAA	mΩ·mm²					
BVdss	V					

Excerpt from the report (4)

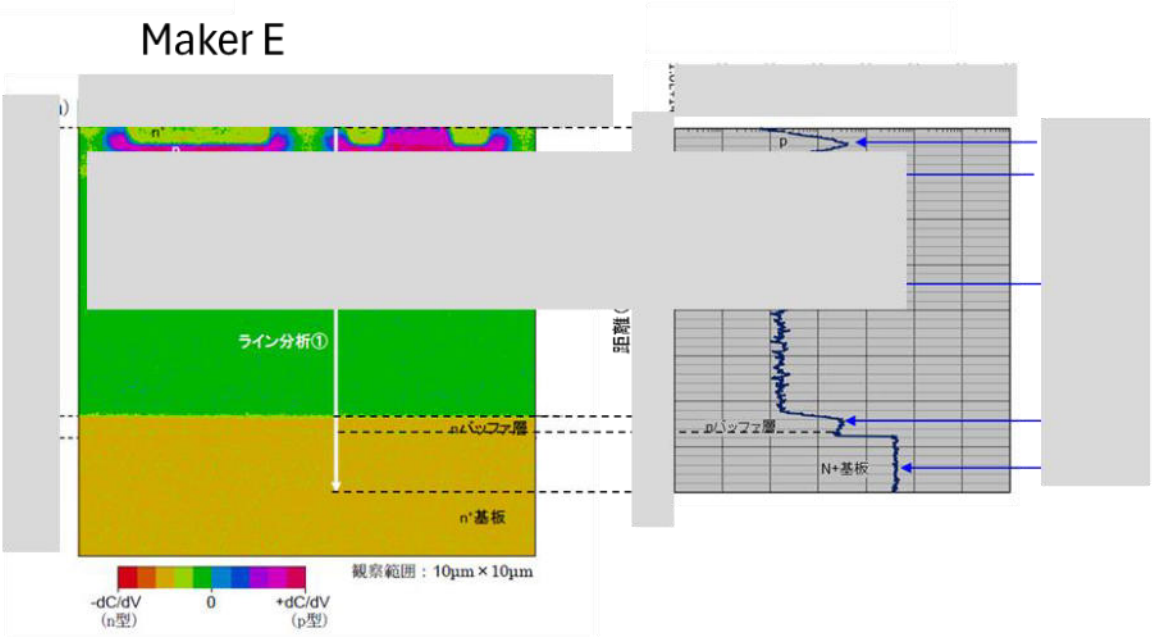
Examples of SCM analysis data

Maker D



Carrier concentration （ Line profile ） and SMM image alignment.

Maker E



Carrier concentration （ Line profile ） and SMM image alignment.